Available online at http://www.csjonline.org/

The Caspian Sea Journal
ISSN: 1578-7899

Volume 10, Issue 1, Supplement 4 (2016) 515-524

Design of a New Flash ADC in 65 Nm CMOS Process

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ABSTRACT─ A new 4bit, 20 GS/s Flash ADC with 2.32 FOM coefficients is presented. Numerous techniques are used to improve overall performance of proposed Flash ADC. Novel comparator is designed that it's created new way to improve performance of Flash ADCs. In addition, averaging technique, MCML circuit, effective capacitance, Transistor sizing and domino logic is used to reduce offset of comparators and then speed up hold system of proposed flash ADC. The new flash ADC consumption only 102 mW at 20 GS/s. the measured ENOB is 3.57 and the layout is embedded by Micro wind software with die area about 0.42×0.42mm2 . The predicted performance is verified by analyses and simulations using HSPICE tool.
Key word: flash ADC, Comparator, preamplifier

Introduction

Ultra-fast electronic systems to convert analog signal to digital is needed in applications such as ultra-wideband (UWB), K-band and satellite receivers [1]. Existing analog to digital converter (ADC) is designed to a specific request which put emphasis on certain parameter that is power dissipation, sampling rate or resolution but puts least deliberation on others [2]. K-band receivers operate up to 12.5 GHz. At this frequency, the receiver demands a high conversion time. Between all ADCs, the best candidates to fit the requirement are Two-step Flash ADC and the Flash ADC. In this work, flash ADC is Candidate to design. The power dissipation of a CMOS flash ADC is relational to the square of the supply voltage, current source and number of transistor that uses in any design; hence, reducing these parameters is the most effective way to reduce the power dissipation. On the other hand, supply voltage and current source reduction and high-sampling rate operations are incompatible. However, it is essential to select a suitable flash ADC architecture. The comparator is a key component of a flash ADC. Sampling rate, resolution and power consumption of a flash ADC directly depend on ability of comparators that used to design flash ADC. Hence, it is important to design high performance comparator. Note that, speed, resolution, linearity and power consumption are critical parameter to design comparator and flash ADC. Therefore, flash ADC offers the highest speed but to design such converter needs a trade-off between those parameters. Optimization to obtain the best portability amongst all parameters enables greater figure of merit (FOM) with the highest performance. FOM is the best parameter to review a flash ADC. Therefore, in this paper flash ADC design approach is to reach to best point of FOM coefficient.

In this research, in section 2 is planned the design approach of flash ADC. In Section 3 is explained and designed flash ADC architecture. Flash ADC consist of different block that speed up of flash ADC depend on speed and performance of each block. Several technique and method are used to improve pre-amplifier, comparators and hold block of flash ADC. A novel structure is also suggested to achieve the overall high performance for the comparator. The comparator design combines various techniques to lower its power dissipation and improve its overall performance.

Section 4 shows results and discussion, and finally Section 5 is the conclusion. Note that, some simulation result and diagram that extract from simulation is placed in section 3.

Flash ADC design approach:

There are numerous ways designing ADCs based on applications. Some ADCs are designed for accuracy, which need high number of bits. Portable device requires low power dissipation, while real-time applications need high speed ADCs. In specific applications, the ADC needs to be high precision and high sampling rate while maintaining low power dissipation. With designing instead of one objective in mind, the design combines several significant functions of the ADC. Figure of merit (FOM) is a quantity used to describe the performance of ADC. To quantify is

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the balance between several functionality that is precision, speed and power consumed. FOM for analog to digital converter takes into account sampling rate, power consumption and resolution. It has units of energy, and represents the energy used per conversion step.

$$E = P/(2^N.F_S) \quad (1)$$

where N is the stated number of bits, *P* is the power consumption and F_S is the sampling rate or speed. Another equation of FOM proposed by Walden et al. (1994) that uses the effective number of bits (ENOB), instead of the stated number of bits[3].

$$FOM = (2^{ENOB}.F_S)/P \quad (2)$$

Based on function (2), sampling frequency will not considerably affect the FOM, but the frequency must able to be worked in K-band. As the ENOB is exponential in manner, having high ENOB will quite especially increase the FOM. Also, as the power dissipation sets lower it will similarly significantly increase the FOM. Figure 1 illustrations a block diagram of a Flash ADC. The figure can be divided into three parts, mainly input reference voltage network, comparators and digital block. Therefore, the first part is to compare the input signal with a reference voltage that it's important to keep the reference voltage fixed or increase in noise will result which in turn decreases the ENOB. To keep the power dissipation low, the whole block of preamplifier, comparator and output logic are kept as simple as possible. In addition, to reduce the effect of deviation in the reference voltage, the input reference voltage network is designed to be in fully differential structure. Therefore, this structure is well-known to be better than a single structure which is prone to be affected by deviation in voltage reference.

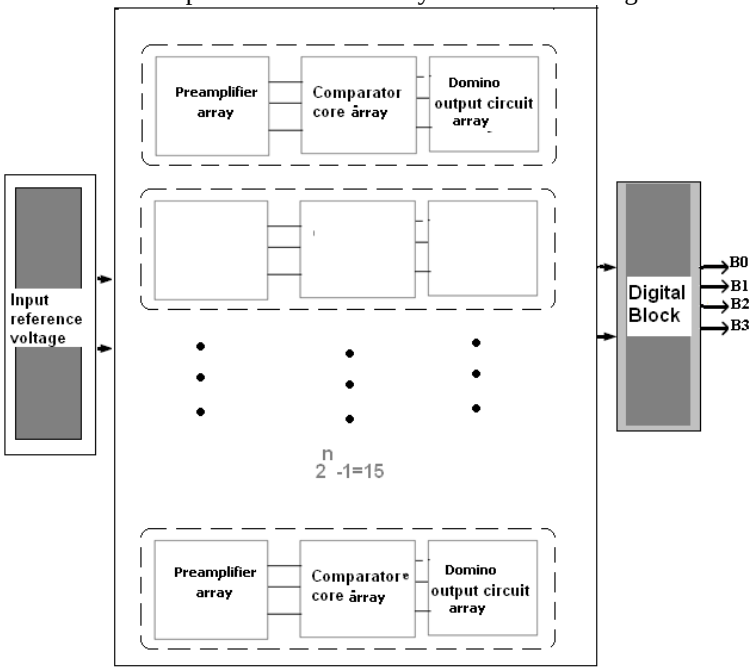

Figure1: Simple block diagram of flash ADC

The design of the comparator must be as simple as possible by removes cascade amplifier and eliminating the active load. Even though the passive load will increase the power slightly but it will increase the speed meaningfully by decreasing the delay and removing the parasitic capacitance effect. Also Passive load has incomplete swing which decreases the regeneration time but require different output logic network. For example when the regeneration is reduced, this will significantly increase the comparator speed. Moreover, the output logic should be stimulated with incomplete swing voltage that is created by the comparator. Output logic is connected to digital block of flash ADC,

as a result shall drive the big load of digital block (decoder) by complete swing voltage (full headroom voltage). Sampling rate of comparator and ADC is directly affected by switching speed of output logic. Moreover, output logic should have complete headroom voltage, high accuracy and high speed as far as possible.

FLASH ADC ARCHITECTURE

Here, the selection way and design of different blocks in ADC as well as and issues related to them are described. Figure 2 shows the role of flash ADC in a K-band system. The gray section is the suggested flash ADC where its block diagram is illustrated in Figure 2.

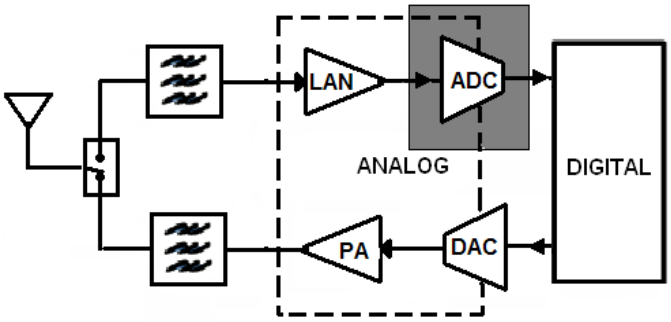

Figure 2: Flash ADC in a UWB and K-band system

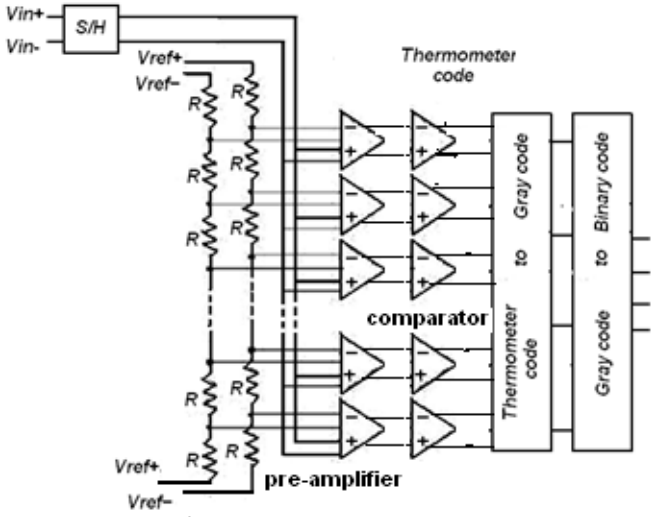

Figure3: Schematic diagram of 4 bit flash ADC architecture

Here, the analog section consists of resistors ladder, pre-amplifier, averaging resistor and comparator core. Also the comparator consists of the output circuit to be connected to the digital section. As known for an "*N*"-bit converter, the circuit employs 2^N-1 pre-amplifiers and comparators. A 4-bit flash ADC architecture has a typical structure which consists of sample and hold, differential ladder network, comparators and digital part end. Although the architecture seems to be a typical structure, some improvements and modifications are done in order to increase the capability of the ADC. For instance, preamplifier uses a passive load in order to decrease headroom voltage which is able to reduce delay and regeneration time between preamplifier and comparator. Therefore, instead of a full swing in the output as in typical complete headroom voltage, the incomplete swing requires a different type of output circuit. In addition domino logic in the output logic is able to translate the incomplete swing to a logic level for the digital block. Another point of modification is discarding the calibration system to eliminate offset, as the calibration

circuit is complex and consumers huge amount of power [4]. For the reason that the block is repeated 2^N-1 time, any reduction in power dissipation will cause in a huge effect in the overall power dissipation. Also the optimization of the parameters is done by applying superposition theorem to maximize the effect of each parameter. Therefore superposition combines the effects by varying each parameter with the other parameters remaining constant. Although full optimization is not achieved, some relationships between parameters as given in Figure 4 are found. The figure illustrates interrelationships in designing a comparator.

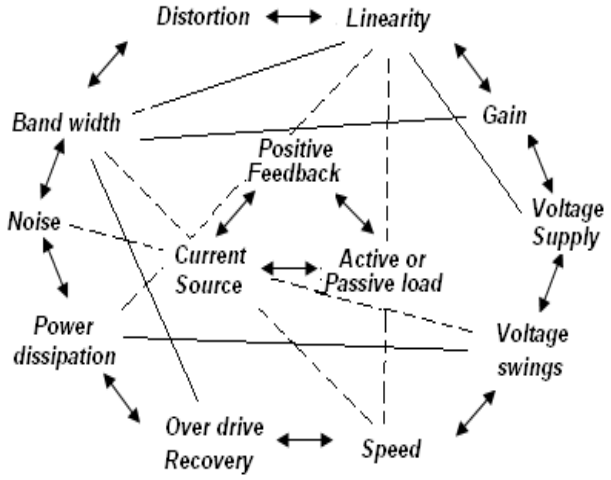

Figure 4: Relationship between comparator design parameters

According to Figure 4, superposition enables the author to careful balance of the trade-off amongst parameters as the trade-offs present many challenges in the design of high quality comparator for flash ADC. Therefore, these trade-offs require intuition and experience to arrive at an acceptable cooperation.
In the digital design stage MOS Common Mode Logic (MCML) is used with certain buffers and dynamic logic. The encoder first converts the thermometer-code into Gray-code, and then generates the respective binary code. Note that Gray-code encoding can also greatly improve metastability. Flash ADCs able to reach the higher sampling rates, with the comparator limiting the maximum achievable. Different techniques to improve the performance of the ADC are proposed at each of its blocks.

A- Ladder network

Ladder network is the first stage of the analog section after the sample and hold (S/H) block [4]. The main role of ladder network is providing reference voltages for the preamplifiers. Because of large number of preamplifiers connected to ladder network nodes, some offset are always present which enforce voltage deviation from assigned value to the ladder network nodes voltages. As result INL and DNL errors will be increased in flash ADC. Note that, a ballast capacitance (27fF-75fF) is used to reduce reference voltage deviation at each tap. Therefore, this technique plays an important role to remove charge injection before preamplifier. Hence, using a ballast capacitance is an effective technique to reduce thermal noise (at high frequencies) in the ladder network.

B- Pre-amplifier

The preamplifier circuit is from MCML families and this amplifier is used in the first stage of flash ADC. First stage of Figure 5 shows proposed preamplifier. Any error, offset or noise in this block will cause errors and problems in all other blocks. Hence, parameters of this part such as, offset, noise, linearity and BW have direct effects on performance of the whole system. Note that, different points need careful consideration in the pre-amplifier design. The pre-amplifier should be as linear as possible. Otherwise, third harmonics are generated which subsequently produce distortion and result in hampering the performance of the flash ADC as a whole. The higher the bandwidth, the lesser the distortions. Furthermore, increase in bandwidth speeds up the pre-amplifier which reduces overdrive recovery, but on the other hand, increases the power dissipation. With instance constant bandwidth, increasing the

bias voltage (V_{gs}-V_t) of the pre-amplifier decreases the output distortions. Also, by increasing bias current and selecting large size transistors (W), the pre-amplifier's offset reductions significantly.

C- Comparator Core:

The second stage of Figure 5 shows comparator core schematic. The load is formed by a series combination of an inductor and a resistor. The differential analog inputs signals are Vp and Vm from the preamplifier. Hence, it has input differential pairs (M_1 and M_2) that turn on when the clock is low and track the input from the previous stage. During the clock is high, the comparator goes into hold mode. In this paper CMOS positive feedback is used to increase the speed of comparator and decrease the regenerative time in latching mode. To achieve best performance, the behaviour during the reset, tracking and regenerative phases should be considered

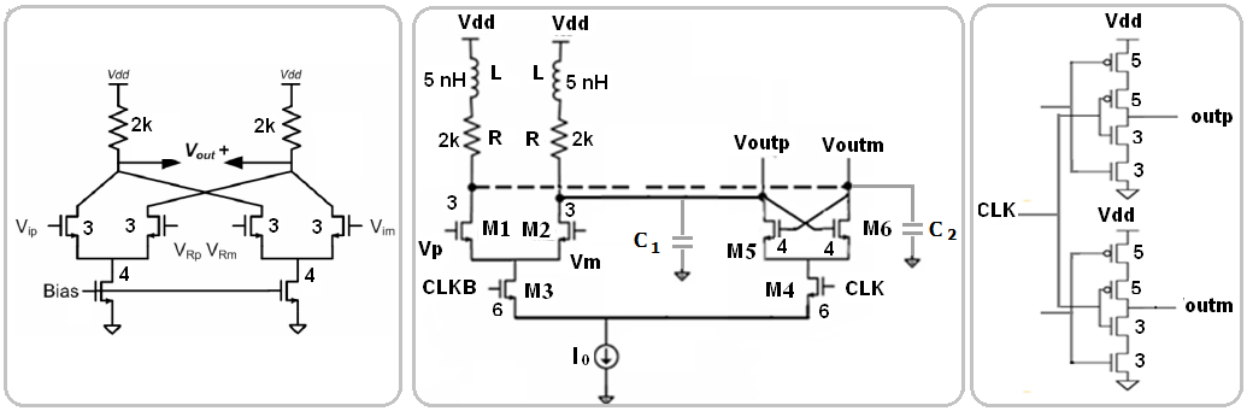

Figure 5: shows comparator schematic that consist of preamplifier, comparator core and output circuit.

In addition, the passive inductor peaking technique is also employed in the T/H circuit to increase the bandwidth. Note that a nonzero inductance decrease the regeneration time, and a more detailed analysis shows that the regenerative time constant reductions monotonically with L. Hence, the largest possible inductance is preferred [5]. Furthermore, for high speed operation, there is a trade-off between speed and power consumption. By increased supply voltage and current source, linearity and speed will go up but power dissipation is a big penalty. The domino output circuit as shown in third stage of Figure 5 is used in place of SR Latch to support the comparator in high speed operation. Therefore, the combination of T/H and output circuit creates a fast structure for the comparator. Note that mismatch was an important attention when using the 65 nm technology to design the comparator, hence careful sizing of transistors helps to mitigate these errors. Different techniques are used to go up the speed of comparator core. One of those points is inductance effect. So a pair of inductances (L1 and L2) integrated into the first comparators structure, also increasing the bandwidth (in amplifying mode), reduce the recovery time constant in latch mode resulting in a faster circuit. The relation between recovery time constant and capacitance transconductance is [5]:

$$\tau = C_{tot} / g_m \tag{3}$$

$$\tau(L) = C_{eff} /(g_{m3,4} - 1/R_{eff}) \tag{4}$$

After adding the inductance, the time constant is justified in Equation (4), where the effective resistance R_{eff} and effective capacitance C_{eff} are:

$$C_{eff} = C - \frac{L}{R^2 + \omega^2 L^2} \quad (5)$$

$$R_{eff} = R + \frac{\omega^2 L^2}{R} \quad (6)$$

Note that, by adjusting the inductance in a way to reduce the time constant of latch recovery, the circuit (latch) will reach a high gain in a short length of time. Current source effect is another point to improve performance of comparator core. The volume of current supplied by the current source has a direct effect on the speed of comparator. One of the factors making this comparator core structure fast is their incomplete output swing as a Figure 7. The output common mode voltage is set close to Vdd/2. Simulation results shown this value offers best performance and can switch to its low and high values fast enough. When clock is low, this stage is in track mode and when the clock is high, the comparator is in latch mode. A high gain and amplification of this stage is not expected and these features will be provided by the second stage (previous stage), as a result the required overdrive recovery time is short. Another point to make here is that the larger the resistor load the larger are the gain, though it will limit the speed. The maximum and minimum rates for this resistor are defined by the time needed for charge and discharge of the total output stray capacitance. New domino logic is purposed in place of SR latch to improve performance of comparator. Domino logic is able to reduce meta-stability errors and speed up the comparator to a range up to 20 GS/s. Capacitance effect is one of the important techniques in this research. Another novelty item that used to design new comparator is integrated c1 and c2 capacitance in front of positive feedback according to Figure 5. There are several reasons and motives to use this technique. First advantage is eliminated effect of the clock feed-through noise from output signal of comparator core. Second advantage is removed switch charge injection to output circuit in the high speed operation of the comparator. Note that, Clock feed-through and channel charge injection is two parameters of switch non-idealities. Third advantage is decreased KT/Q noise. Another advantage is reduced switching resistance in triode region and finally speed up operation of proposed comparators. Figure 7, 8 shown output signal before and after integrated c1, c2 capacitance. According to second stage of Figure 5 c1 and c2 was important effect to improve output signal of comparator.

D. Averaging Technique

Averaging technique was used to degrade static errors, offset errors, and the INL and DNL errors [4]. In addition, this technique also improves SNR without any extra power dissipation. The weaknesses of this technique are bandwidth reduction and also increase in the die area. In this work, an averaging resistor (R_{ave}) was connected to the preamplifier's output as a loop and by varying its value through simulation using H-Spice then the best resistance value was defined. Figure 4.3 shows the offset in terms of the ratio of R_{ave}/R_L. The curve shows that the offset is minimum point for the ratio of 3.5 and above 4.5 the offset gets worse.

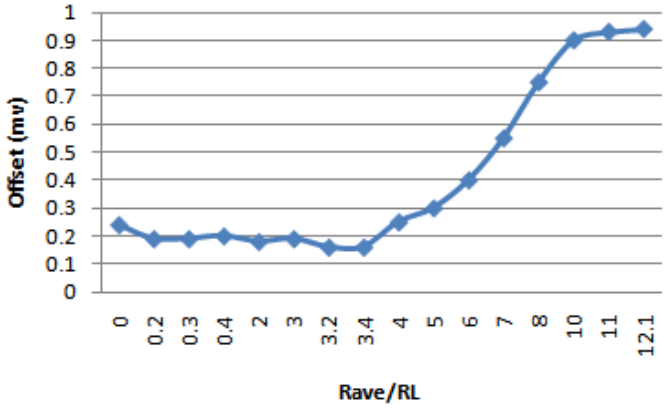

Figure 6: The offset in terms of the ratio of R_{ave}/R_L

Results and Discussion

In this work, the flash ADC and all its stages such as ladder network, pre-amplifier, comparator are designed and simulated by different software's. The improved performance of the Flash ADC due to the proposed techniques is verified based on the simulation results. In addition, the performance of the circuits in terms of speed, power dissipation, linearity and ENOB are also analyzed and discussed. The most important block of the flash ADC is the comparator core. This block should response to digital section with a high sampling rate and accuracy. Therefore, parameters such as current, inductance, and the size of transistors should be determined in a way that the input signal is amplified enough to provide a suitable voltage level for the digital block. Note that all this most do with respect to characteristics and features of comparators, the bigger the inductance, the lower the regeneration time and the higher the speed of the comparator. But in practice, due to issues such as non-ideal characters and the limited volume of large inductances, the size of the inductance cannot be arbitrarily large. Simulation results exposed that a sufficiently small inductance can be used while keeping the regeneration time to the desired value. Furthermore parameters such as gain, speed and offset are importance in the design of the comparator block. As shown in Figure 7 output wave of the comparator core is not symmetric and ideal. There is some spurt wave on the output signal of the comparator core that injected from clock. These phenomena called effect of clock feed-through. Clock feed-through is sources of offset and noise in the comparator core. When comparator core operate in high speed range, effect of clock feed-through coupled to output of the comparator. As result, accuracy of circuit decreased and then SNR, SFDR, ENOB parameter reduced. Therefore, comparator core is not able to work in proposed high speed range. Hence, in this research C_1 and C_2 capacitance suggested to improve output signal of comparator core and as result speed up of this circuit. When we have a symmetric wave in output of the comparator, therefore, probability of error is coming down. Figure 8 shown effects of C1 and C2 capacitance on output signal of the comparator core.

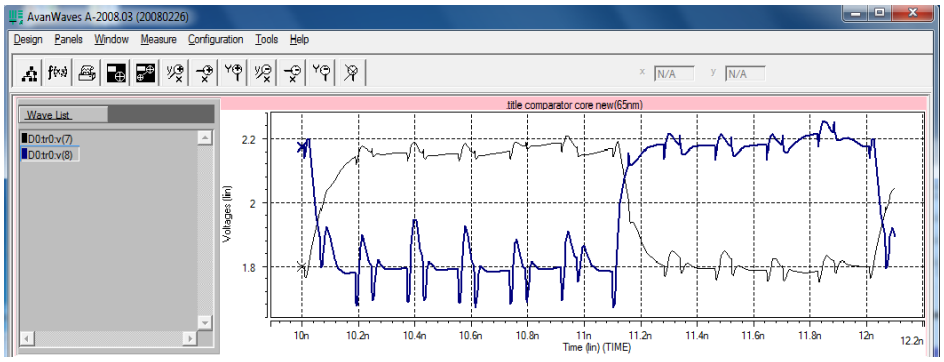

Figure 7: output signal of the comparator core without c1 and c2 capacitance

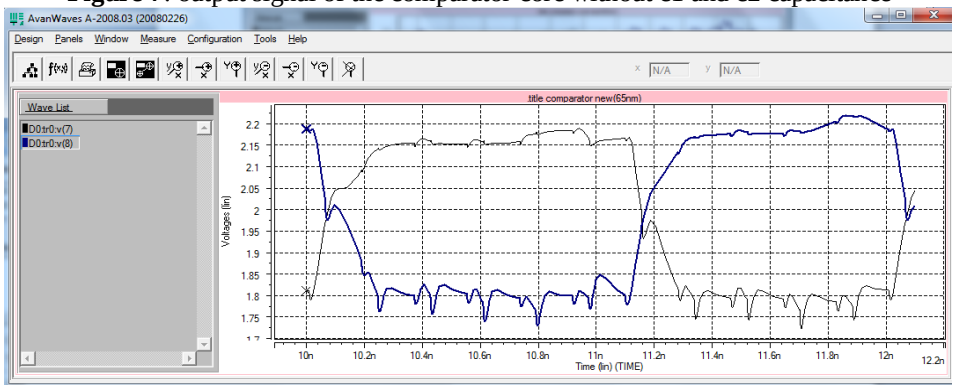

Figure 8: output signal of the comparator core with integrated C1 and C2 (C=20Ff) capacitance.

Simulation results revealed that the comparator core alone cannot stimulate the digital section in speeds higher than 5 GS/s. On the other hand, this block cannot provide the load required in the digital stage in such high speeds.

Hence, a high performance circuit in front of positive feedback is required to drive the load of the digital stage and at the same time does not generate extra offset before the comparator. The suggested solution is the usage of a domino logic as the comparators output connected to the digital section. According to Figure 9 simulation presented that the proposed structure can increase the comparator's speed up to 20 GS/s and the digital section can still be switched. In addition, the FFT frequency response is used to determine the SFDR, SNDR, EONB and SNR values.

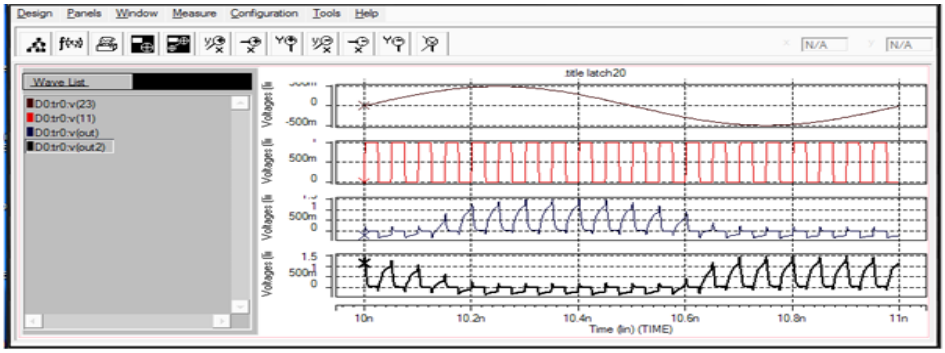

Figure 9: Output wave of the proposed comparator, F_{in}=1 GHz, F_{clk}=20 GS/s.

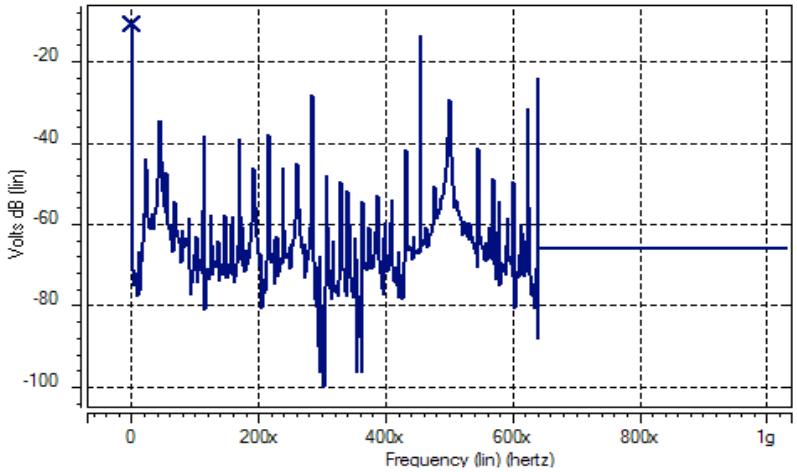

Figure 10: FFT diagram of the comparator at input frequency of 6.5 GHz and sampling rate of 20 GS/s.

After improvement of different blocks such as comparator core, preamplifier and other stages, the flash ADC was assembled. In this research, a 65 nm CMOS flash ADC for high speed, low power and K-band application is proposed. The maximum sampling speed is 20 GS/s and the SFDR at 1 GHz is 12.71 dB. The supply voltage is only 1.8 V. in addition, several design issues which have been discussed before are used in the optimization. CMOS positive feedback, (C1 , C2) capacitance effect and a new structure based on domino CMOS logic as output circuit are used to develop sampling rate and performance of the comparator. Furthermore, the measured ENOB is 3.57 bits at 20 GS/s with a 1 GHz sinusoidal wave input signal. Table 1 presents comparisons between suggested flash ADC and designs in previous papers. Note that the sampling rate of proposed comparator is more than 20 GS/s while sampling rate of proposed flash ADC is only 20 GS/s. Also, Fast Fourier Transform (FFT) is performed to observe the dynamic characteristics such as the ENOB of the comparator. Figure 11 illustrates FFT of flash ADC at input frequency of 2.5 GHz. The new flash ADC dissipates only 102 mW at 20 GS/s. Transistor sizing technique has been used to optimize die area, power dissipation, delay and speed up of the flash ADC. Also, FOM is an important factor to show quality and performance of ADCs. In addition, the proposed flash ADC has been found have to the

best FOM factor when compare to previous works. Figure 12 illustrates layout of the flash ADC. The proposed layout of flash ADC resulted in a die area is about $0.42 \times 0.42 mm^2$.

Table 1: Performance comparison is between proposed flash ADC and previous papers.

Reference	Speed (GS/s)	Voltage (V)	ENOB	Process (nm)	Power (mV)	year	Analysis	FOM
[10]	3	1.8	4.7	65	39.4	2013	Simulation	1.7
[13]	1.2	1	5.3	90	40.5	2008	Simulation	1.102
[6]	1.6	1	5.58	65	29.1	2015	simulation	2.6
[9]	4	1.8	3.4	180	68	2007	Simulation	0.713
[7]	7.5	-	3.8	65	15.3	2015	experimental	2.04
[12]	10.3	0.9	5.3	40	242	2013	Simulation	1.67
[11]	2.4	1.8	3- 5.1	90	28	2014	Simulation	1.41
[8]	0.08	1.8	4.65	180	0.9	2015	Simulation	2.23
This work	20	1.8	3.57	65	102	2016	Simulation	2.32

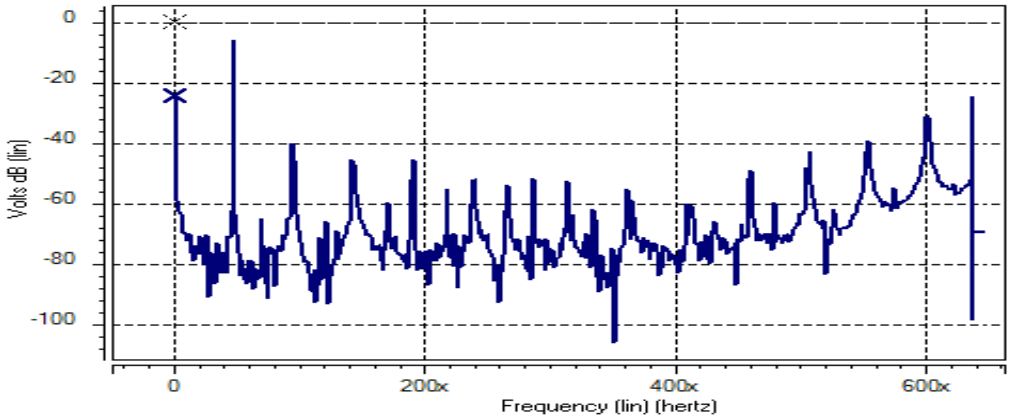

Figure 11: FFT of the flash ADC at input frequency of 2.5 GHz and sampling rate of 7 GS/s

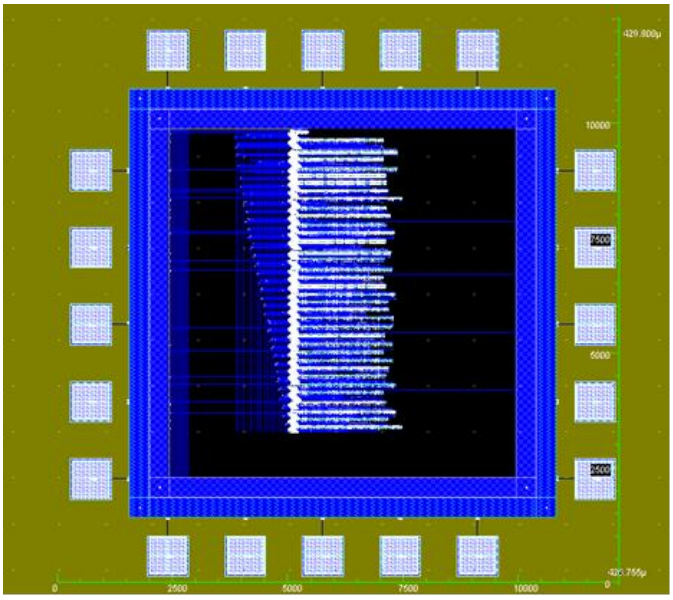

Figure 12: Layout of the proposed flash ADC

Conclusions

In this paper, a high speed flash ADC is designed using several stages, consisting of ladder network, preamplifier, comparator and digital section. The whole system was simulated using H-spice software to verify the workability of the newly developed flash ADC. Therefore, a 20 GS/s comparator in 65 nm CMOS technology is designed which to date is one of the fastest comparator achieved. This comparator opens the way to design flash ADC with a range up to 20 GS/s which should be needed for UWB and K-band applications. Simulation results in 65nm CMOS process shows that it is possible to design a flash ADC in a range up to 20 GS/s by optimizing the design of comparator, pre-amplifier, ladder network and digital part. The layout of flash ADC is designed by Micro wind software with a die area about $0.42\times0.42\text{mm}^2$. The measured of ENOB is 3.57 bit, with power consumption of 102 mW and 2.32 FOM. This achievement is beneficial for high speed system especially in UWB and K-band applications.

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