

## Simulating, Prototyping, Designing and Replacing an Unmoving Converter on Air Vehicle

Thomas Sivasankaran

Department of Mechanical Engineering, University of Malaya, 50603 Kuala Lumpur, Malaysia

**ABSTRACT**— The present article provides simulation, design and engineering of an unmoving converter or inverter in place of a moveable inverter on aero plane. The inverter is allowed for 1 kVA formal power and 400 Hz, three-phase, 36 V sinusoidal output voltages whereas the input voltage is 27 V dc. The dimensions of the inverter due to some constraints in the space of installation and weight must be least possible. This needs transformer dimensions to be reduced by the increase of switching frequency. It motivates the losses to heighten and to decrease the losses and guard the switching transistors; it needs to design snubber circuits. Moreover, by engineering digital PID controller, the control unit of moveable inverter is removed from the air vehicle. The privilege of this inverter is that its output voltage adjustment has been made stable and the THD is less than three percent. Removal of the 3-p transformers and decreasing the dimensions of output filters are the other privileges of this converter. The outcome of this research results in producing of prototype inverter that has been examined from operation perspective.

**KEYWORDS:** static inverter, digital control, snubber circuit, switching, push-pull

### Introduction

Today, with regards to the sanctions imposed on the country, and necessity of overhaul and maintenance of aviation systems for self sufficiency in specialized fields, it seems necessary to design successor systems and native respective technology. Among aviation systems is dynamic inverter system (motor-generator) which is rated for 1 kVA nominal power and 400 Hz, three-phase, 36 V sinusoidal output voltage. This inverter supplies the navigation and sight systems on aircraft. The input voltage of this inverter is 27 VDC which is provided by the aircraft DC generators or aircraft batteries and rotates the shaft of a DC rotor with the speed of 12000 r.p.m. and induces a 3-phase, 36 V, 400 Hz voltage in the stator of an AC Generator. Regulation and control of the inverter output voltage is handled by a unit apart from aircraft dynamic inverter, by the control field current method in the DC rotor. With regards to the old design of the system and introducing various problems and defects (the defect of bearings and brushes and some other mechanical failures), it is required to replace this inverter with a newer static system with digital control as well as a fast diagnostic system by LED displays. The initial driving current in the dynamic inverter is more than 170A, but for the static inverter, it reduces to less than 8A and because the design is fully native, it's possible to optimize any possible changes proportional with feature needs.

### Inverter design

Dynamic inverters (motor-generator systems) are the first generation inverters. As time passes, various needs were encountered and by increasing the semiconductors transfer speed, static inverters was constructed in switching method and then by using the properties of ferromagnetic materials, resonance inverters were produced. With the advancement of technology in the semiconductor devices and digital processing controllers, the PWM and SPWM modulation were utilized. In this inverter in the DC-DC power block, the PWM modulation with the carrier frequency of 16KHz is used, while in DC-AC block the SPWM modulation with carrier frequency of 18 KHz is used. Fig.1 shows the static inverter block diagram .

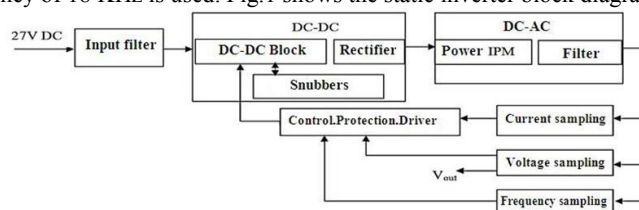


Fig.1.static inverter block diagram

The static inverter principle was based on the power IGBT transistors high frequency PWM and SPWM modulation [1,2]. The input line filters prevents the RF radiation and noise and spikes to the main DC bus. This is a low pass filter which is composed of two inductors and one capacitor. Fig.2 shows the line filter.

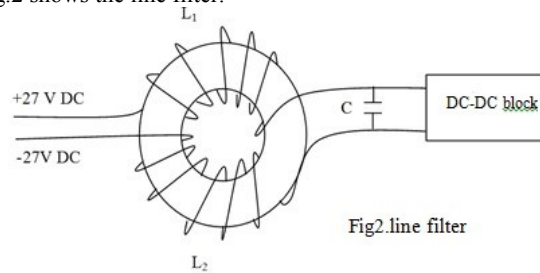


Fig2. line filter

It should be mentioned that the direction of windings of the inductors on the troids are opposite of each other to appear as a noise attenuator. The inductor values of L1 and L2 are equal. The 27VDC signal which supplies from aircraft batteries or DC generators applied to the DC-DC block. This signal, after passing through DC-DC block, increase to 65 VDC and supplies the IGBT transistors in the IPM(intelligent power module) block[3]. In order to increase the voltage level, we use ferrite transformers with high permeability in high frequency. With this approach, in addition to isolating the input blocks from outputs, the need to 3-phase transformer is removed and the required voltage is produced in smaller space[4]. In order to control or protect the output voltage, the sampler blocks of current and voltage and frequency, apply the sampled signals to the control and protection block. The control protection block protects the inverter against the short circuit and overvoltage and over current.

**2.1.DC-DC Block**

The topology used in DC-DC block is the Fed current push pull(Fig3). In this topology, the fed current transformer increases the output power and reduces the push pull unbalances. The advantages of this topology like flyback and bridge is that the energy is not reserved in the transformer coil and the current in the secondary flows simultaneously with the conducting of respective transistors in the primary. The working time of each transistor is equal to half of main frequency so that limitation factors such as heat and noise reduces to half [5,6]. The elements of this block are the push pull transformer and IGBT transistors and rectifier diodes. The snubber circuits in this topology, protect the IGBT transistors against the voltage spikes and decrease the losses.

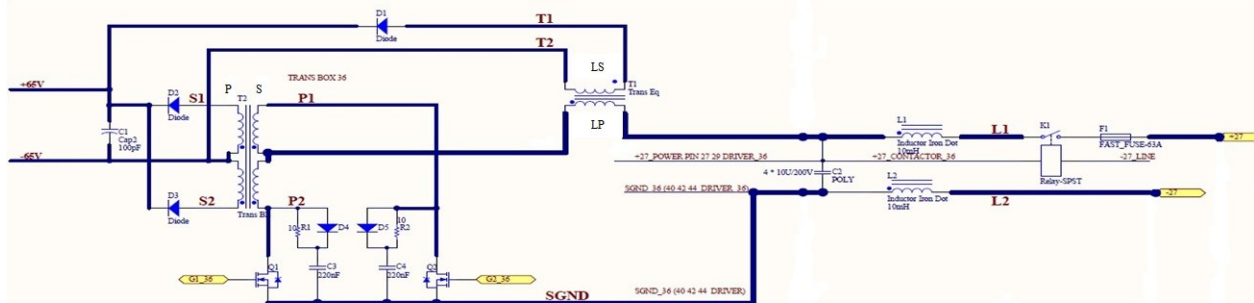
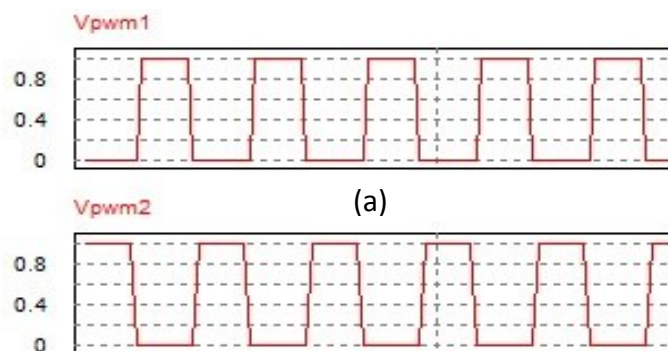


Fig.3 DC-DC block

In this block the diode "D1" is the fed current feedback diode and "D2" and "D3" are the rectifier diodes. The coupled inductor "L1" and "L2" and parallel capacitor "C1" are the elements of a noise filter.

In this topology, when either Q1 or Q2 transistors switched on, the voltage over half-trans secondary is  $V_o + V_D$ . Hence the voltage of primary tab ( $V_{ct}$ ) is  $N_p/N_s(V_o + V_D)$ . The ratio of  $N_p/N_s$  is selected such that  $V_{ct}$  is 25% less than that lowest ripple of the input voltage. By switching each transistor on, the dotted head potential of the primary of the fed current trans(NLP) becomes negative and the current flows through the push pull trans center tab. By switching the transistor off the dotted head of (NLP) trans becomes positive and D1 conducts through the output voltage and supplies the current to the output.

The diagrams "a" and "b" show the waveform of PWM switching frequency and the diagrams "c" and "d" show the collector-emitter voltage waveforms and reduction in the voltage variation by this topology which simulated by PSIM software. In order to prevent "skin effect" in high frequency conducting, we use "Litz" parallel bundle wires. The ramped waveform of transistors current in diagrams "e" and "f" represents the reduction of current drawn by the transistors in this topology [7,8].



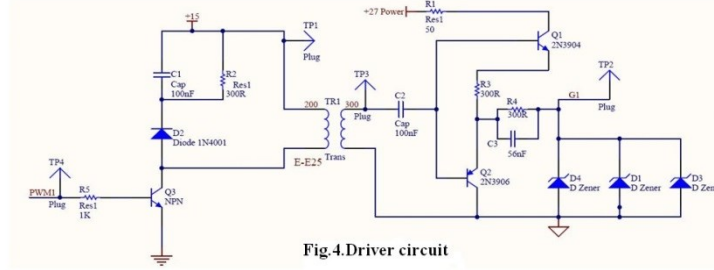
In the DC-DC block , in order to protect power transistors, we use RCD snubbers which composed of resistors R1 and R2, capacitors C1 and C2 and diodes D1 and D2.

If the switching frequency is 16 KHz and each transistor switched off during 700 nanoseconds, the RCD snubber specifications in this inverter should be according to formula 1 and 2.

$$R_1 = R_2 \leq \frac{t_{on} (min)}{5C} \cong 10 \Omega \quad (1)$$

$$C_3 = C_4 = \frac{t_{off} \times I_L}{2V_m} \cong 220 \text{ nf} \quad (2)$$

The main purpose of the DC-DC block is to increase the DC voltage level to 65 VDC so that in no load and full load output, the DC voltage level remains constant[9,10]. In this inverter only the DC-DC output voltage is controlled and regulated. This regulated voltage is applied to the IPM block which generates 3-phase,36V,400 Hz voltages. In the driver part (Fig.4), the PWM pulses, first isolated from input parts (by optocoupler transistors) and then are amplified by transformers and protected with zener diodes and applied to the gate of IGBT transistors[11].



In this circuit, when the transistor Q1 switched on, the capacitor C3 speeds up the transfer rate of gate voltage pulses and when the transistor Q1 switched off with the resistor R4, evacuated the charge voltages via transistor Q2 as a RC snubber

## 2.2.Inverter block

This block is a DC-AC convertor and include two main parts: power IPM part and output filter. The power IPM module was formed of six IGBT transistors in the 3-phase bridge configuration. The IPM module converts the 65 VDC to 3-phase, 36V, 400Hz voltage. The inverter output rms voltage (VL) calculates according to formula 3 , 4.

$$V_L \cong 0.612 \times m_a \cdot V_{DC} \cong 36 \text{ V} , m_a \cong 0.95 \quad (3)$$

$$V_L = \sqrt{3} \times \frac{(V_{PH})}{\sqrt{2}} = \frac{\sqrt{3}}{2\sqrt{2}} m_a \cdot V_{DC} \cong 0.612 \times m_a \cdot V_{DC} \quad (4)$$

Where VPH is the phase voltage and VDC is the DC-DC block output voltage and ma is the modulation index. In this inverter, by using the SPWM modulation and increasing the carrier frequency, harmonic distortion decreases and low level harmonics are eliminated and output filter dimensions decreases [12,13]. The specification of output low-pass LC filter is obtained according to formula (5) , (6) , (7)

$$L = \frac{\sqrt{2} R_L}{W} \cong 100 \mu H \quad (5)$$

$$A_L \cong 40 , n = \sqrt{L(nH) / A_L} \cong 50 \quad (7)$$

$$C = \frac{1}{R_L W \sqrt{2}} \cong 10 \mu f$$

Where, AL is the coil inductance (nH) in 1000 turns and n is the number of coil turns.

## 2.3.Control, Protection, Driver block

This block generates the PWM and SPWM pulses and regulates the DC-DC block output voltage and protects the system against output over voltages and over currents. All of this commands are issued by two microcontrollers.

A PID digital controller is made by one of this microcontrollers[14].By increase the output loads, the PID controller decrease the pulsewidth modulation so the DC output voltage level remains constant.[15,16]

## 3.Simulation and Results

Fig.5 shows the open-loop transient time response of the DC-DC block output voltage simulated in PSIM. The time constant  $\tau$  is about 20 miliseconds. The simulated control loop by PID controller (with a good approximation) is as follows:

$$\tau \cong 20 \text{ ms} \tag{8}$$

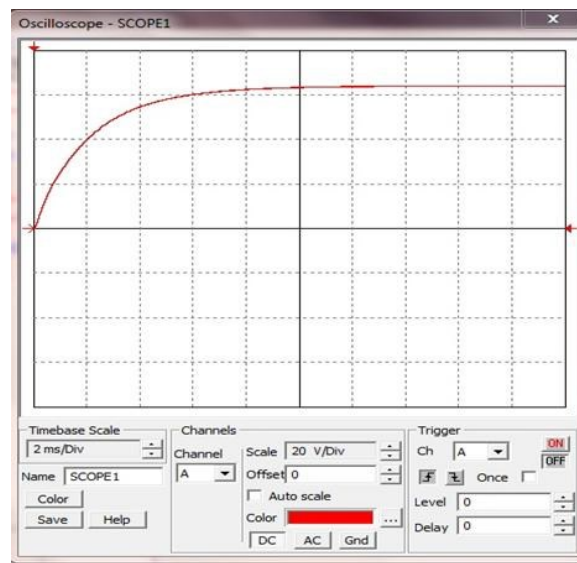
$$G(s) \cong \frac{50}{S + 50} \tag{9}$$

$$H(s) \cong \frac{S + 800}{S + 115} \tag{10}$$

And by sampling rate of 2ms in Discrete area:

$$GH(s) \cong \frac{50 S + 40000}{S^2 + 165 S + 5750} \tag{11}$$

$$H(z) \cong \frac{1614 Z - 166 .7}{Z - 0.7937} \tag{12}$$



**Fig.5.DC-DC output transient time response**

The control block microcontroller is programmed by this formula using the CodeVision software so that in different loads, by adjusting the pulsewidth modulation, the DC voltage level remains constant. Figure 6 shows the closed-loop transient time response, locus of roots and the Bode diagrams in MATLAB. The gain margin is infinite and the phase margin is 60 degrees which are desired amounts and by changing the gain, the closed loop voltage remains stable. Figure 7 shows the THD which obtained from PSIM software simulation. It is about 2 percent and desired in aviation applications. Figure 8 shows the THD obtained from HP-334A distortion analyzer. Figure 9 shows the output voltage signal.

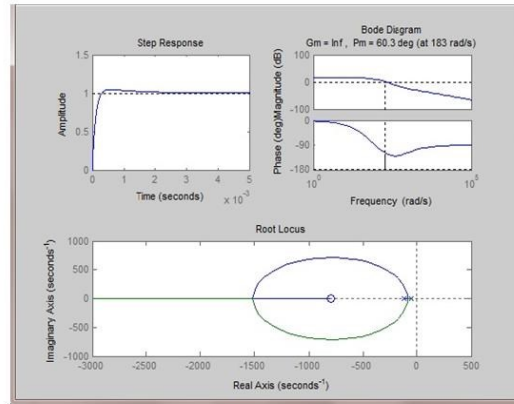


Fig.6. transient time response.Bode diagrams.locus of the roots

THD	
Fundamental Frequency	4.000000e+002 HZ
V <sub>ab</sub>	2.0295189e-002
V <sub>ac</sub>	1.9596006e-002
V <sub>bc</sub>	2.0361328e-002

Fig.7.Simulated THD



Fig.8.Output voltage THD

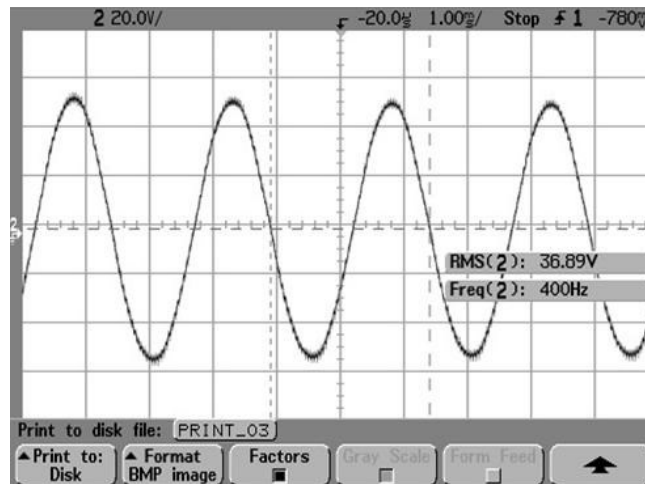


Fig.9. Output voltage waveform

### Conclusions

A three-phase, 400 Hz, 36 V static inverter was designed for aircraft and then it was prototyped. This inverter will replace a dynamic inverter on aircraft. The initial drive current reduced from 170A to 8A. In the design of inverter, because of some limitations in the space of installation, with increasing the switching frequency and use of ferrite transformers, the inverter dimensions were reduced. By the method of control over DC voltage in DC-DC block and applying fully digital controller and SPWM modulation, the output transformers were deleted, the output filter becomes smaller, high frequency harmonics are eliminated and THD reduces to less than 3%. Furthermore, the control unit of dynamic inverter was deleted from the aircraft and a fully native inverter with the full standard specifications and the capability of easier maintenance was achieved inside the country.

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